REMARKS

By this amendment, claims 1, 17, 26, 48, and 62-64 have been amended. Claims 1-64 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claims 1-13, 17-22, 26-36, 38-49, and 51-64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Curran (US 5,574,921) in view of Devanney (US 6,243,779), and also unpatentable over Bus-Invert Coding for Low-Power I/O by M.R. Stan and W.P. Burleson (hereinafter "Burleson") in view of Devanney. Claims 1, 13-17, 22-26, 36-37, 48, 50, and 63-64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over de la Iglesia et al. (US 6,490,703) in view of Devanney. These rejections are respectfully traversed.

Claim 1, as amended, recites a method of performing bus inversion on first bits to be transmitted on a bidirectional bus from a first device to a second device comprising, *inter alia*, "capturing a state of previously transmitted bits on the bidirectional bus with a first clocked register according to a clock signal, capturing a state of an inversion bit associated with the previously transmitted bits with a second clocked register according to the clock signal, and determining from the captured state of the previously transmitted bits whether the first bits should be inverted" (emphasis added). Claims 26 and 62-64 recite similar limitations. Applicant respectfully submits that none of Curran, Burleson, or de la Iglesia et al. discloses, teaches, or suggests these limitations.

Claim 17, as amended, recites a method of outputting first bits on a bidirectional bus from a first device to a second device "outputting inverted first bits on the bidirectional bus, and outputting on a separate line, with a clocked register according to

a clock signal, the inversion bit with a value indicating that the first bits have been inverted; [or] outputting on a separate line, with a clocked register according to the clock signal, the inversion bit with a value indicating that the first bits have not been inverted" (emphasis added). Claim 48 recites similar limitations. Applicant respectfully submits that none of Curran, Burleson, or de la Iglesia et al. disclosees, teaches, or suggests these limitations.

Curran, Burleson, and de la Iglesia et al. are silent with respect to "capturing a state of previously transmitted bits ... with a first clocked register according to a clock signal" and "capturing a state of an inversion bit associated with the previously transmitted bits with a second clocked register according to the clock signal," as recited in claims 1, 26, and 62-64. Curran, Burleson, and de la Iglesia et al. are also silent with respect to "outputting on a separate line[] with a clocked register according to a clock signal, the inversion bit " or "outputting on the separate line[] with the clocked register according to the clock signal, the inversion bit," as recited in claim 17. Claim 48 recites similar limitstions. Nor is Devanney cited for this limitation, and thus does not cure the deficiencies of Curran, Burleson, and de la Iglesia et al. Accordingly, claims 1, 17, 26, 48, and 62-64 are allowable over the cited combinations.

Moreover, each Curran outputs the inversion bit on the same bus 188 as the data bits. Col. 7, ln. 46-47; FIG. 6. Therefore, Curran does not disclose, teach, or suggest "outputting inverted first bits on the bidirectional bus, and outputting on a separate line ... the inversion bit," as recited in claims 17 and 48.

Furthermore, the Office Action admits that Curran, Burleson, and de la Iglesia et al. do not teach or disclose previously transmitted bits on a bidirectional bus. Office Action at 3-4, 6, and 9. Instead, the Office Action asserts that "it would have been obvious to use Curran's bit inversion on either a unidirectional or bidirectional bus

because this would have prevented limiting the usability of Curran's system," to allegedly arrive at the claimed invention. Office Action at 3. The Office Action makes similar statements for Burleson and de la Iglesia et al. Office Action at 6 and 9. The Office Action has not applied the proper test for obviousness; accordingly, the Office Action fails to make a *prima facie* case of obviousness.

Applicant respectfully submits that there is no motivation to combine the cited references to obtain the invention of claims 1-64. Motivation or suggestion to combine or modify prior art references "must be clear and particular, and it must be supported by actual evidence." *Teleflex, Inc. v. Ficosa North America Corp.*, 299 F.3d 1313, 1334 (Fed. Cir. 2002). Because the "genius of invention is often a combination of known elements which in hindsight seems preordained," the Federal Circuit requires a "rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *McGinley*, 262, F.3d at 1351. Yet there is no teaching or suggestion within any of the references that provide a motivation to combine them.

Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. *See e.g., In re Dembiczak*, 175 F.3d 994 (Fed. Cir. 1999); *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998); *Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.*, 75 F.3d 1568, 1573 (Fed. Cir. 1996); and MPEP §§ 706.02(j) and 2143 *et seq.* Furthermore, the "[t]he teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP §706.02(j).

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). Thus, a showing of an obvious combination requires more than just an amalgam of references, each of which provides one feature of the claimed invention.

The Office Action has done no more than cite a pair of references, each of which allegedly provides only part of the claimed invention, and allege that their combination renders the invention obvious. However, without the benefit of hindsight, there would have been no motivation to combine these references and the Office Action has failed to provide proof of any such motivation.

Since there is no motivation to combine the teachings of Curran and Devanney, or Burleson and Devanney, claims 1-13, 17-22, 26-36, 38-49, and 51-64 are not obvious over the cited references. Furthermore, since there is no motivation to combine the teachings of de la Iglesia et al. and Devanney, claims 1, 13-17, 22-26, 36-37, 48, 50, and 62 are not obvious over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejections of claims 1-64 be withdrawn and the claims allowed.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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